Investigation of Key Technologies for System-in-Package Integration of Inertial MEMS

N. Marenco¹, W. Reinert¹, S. Warnat¹, P. Lange¹, S. Gruenzig¹, G. Allegato², G. Hillmann³, H. Kostner³, W. Gal⁴, S. Guadagnuolo⁵, A. Conte⁵, K. Malecki⁶, K. Friedel⁶

¹) Fraunhofer Institute for Silicon Technology (ISIT) - Fraunhoferstrasse 1, 25524 Itzehoe, Germany
²) ST Microelectronics Srl - Via C. Olivetti 2, 20041 Agrate Brianza, Italy
³) Datacon Technology GmbH - Innstrasse 16, 6240 Radfeld, Austria
⁴) FICO B.V. - Ratio 6, 6921 RW Duiven, The Netherlands
⁵) SAES getters SpA - Viale Italia 77, 20020 Lainate (MI), Italy
⁶) Wroclaw University of Technology - Wybrzeze Wyspianskiego 27, 50-370 Wroclaw, Poland

Abstract: "System-in-Package" is a key concept to achieve minimum size and costs in hybrid integration. We investigated several related technologies for inertial sensor MEMS packaging, with special emphasis on vacuum packaging of resonant devices like gyroscopes: Hermetic Chip-to-Wafer and Wafer-to-Wafer bonding, Through-Silicon Via in thick and in thin wafers, thin-film getter deposition and fine patterning, and full-wafer transfer molding. This paper shows the achievements of the project after finalizing the main R&D activities. Currently, we are attempting the full flow implementation on functional devices.¹

¹ The presented works are results from the DAVID project, funded under the Sixth European Framework Programme (IST-027240) until June 2009.

I. INTRODUCTION

Hermetic waferlevel packaging of MEMS is generally performed using a passive cap wafer and a subsequent bond pad opening step. Today, most industrial companies offer this kind of packaging for inertial sensors - mainly accelerometers, but also gyroscope resonators for angular velocity measurements. The hybrid system is built by wire bonding the MEMS to an ASIC, using adapted versions of package types like LGA, QFN, SOP, etc.

A considerable reduction of size and costs can be achieved by a direct bonding of the MEMS to the ASIC on wafer level, thus omitting the passive cap and establishing the electrical interconnect and hermetic sealing at once. In some
cases, the use of TSV technology is mandatory, in others it can be an interesting option.

If vacuum below 0.1 mbar is required, getter films can be used. The cavity volume in our approach measures only 130 nl and is formed by MEMS structures on one side and a CMOS surface on the other. Therefore we have to deal with outgassing issues, and getter fine-structuring becomes necessary to exploit the available area.

Finally, after the waferlevel packaging, an efficient protection of the system can be achieved by wafer molding. Stress reduction and warpage control are most important issues in process technology and lifetime reliability.

All of these challenges were considered by experimental and theoretical means, using dedicated test vehicles. The integration with functional devices is still ongoing; latest results are to be presented in the conference.

C2W and W2W as two complementary approaches

Our integration followed two conceptually very different ideas: The preferred industrial approach for high volume manufacturing is a Wafer-to-Wafer (W2W) technology, requiring a matched MEMS and ASIC design in terms of die size and wafer format to allow wafer bonding. There are good reasons to think about a more flexible solution: We suggest a Chip-to-Wafer (C2W) concept that is more suitable for smaller volume production and can even allow multi-project wafer use. Our target in DAVID was to show both C2W and W2W integrations, each in a complete process flow, e.g. bonding a resonator MEMS to a CMOS wafer with investigations on vacuum aspects and 2nd level conditioning by solder balling and wafer molding.

II. EXPERIMENTAL APPROACH

Our process studies prior to a functional implementation involved a large amount of work on dummy wafers that reflect as much as necessary the relevant parts of functional devices: Bonding process dummies included daisy chains and a sealframe with a lateral feedthrough underneath. TSV process elements were studied on various test wafers, ranging from simple blind holes to double-side structured wafers with a pre-metal dielectric (PMD) comparable to CMOS products. Large-area molding was first investigated in a 200 x 36 mm² mold with bimaterial strips of silicon and mold compound, before a 6” wafer mold was manufactured. All experiments were closely accompanied by theoretical studies about mold compound properties.

As a functional device for the C2W integration, a MEMS resonator was designed and manufactured with a variety of comb widths / gaps from 0.8 µm to 1.5 µm. Passive test structures allowed to verify the quality of our surface micromachining process "PSM-X2" from Fraunhofer ISIT [1]. For operating this MEMS, a standard resonator driver was provided by ST Microelectronics on 8” multi-project wafers in HCMOSTA technology. We applied a circle cut to 6” format for handling purposes. The ASIC design was only modified by adding a pad extension at the periphery of the die for TSV process development. As a process option, we ordered a thick planarized passivation covering all top metal structures. Getter- and vacuum compliance of the standard CMOS surface finish was studied on an accelerometer driver product, which allowed us to evaluated a significant quantity of circuits on industrial electrical wafer sort equipment.

The integration of the W2W approach was made on a modified accelerometer MEMS and driver ASIC, equally from ST Microelectronics’ product line, but both with considerable design adaptations to fit for the new integration approach.

III. C2W INTEGRATION FLOW

The core component of the C2W integration is a two-step bonding process of single MEMS dies on a full CMOS wafer. A first "pre-fixation" step is performed with ultrasonic bonding. A small gap remains to evacuate the cavity in the final bonding step, performed as a gang process on a modified wafer bonder.

![Figure 2: Our C2W process consists of two steps: MEMS dies are placed and attached on the CMOS wafer using ultrasonic bonding. A remaining gap allows the evacuation of the cavity prior to the final bonding, where the system is permanently sealed under heat and pressure.](image)

In the "pre-fixation" process, we handle open MEMS resonators and therefore require excellent cleanliness conditions to achieve a reasonable yield. Our studies confirmed that the concentration of airborne particles in the die bonder can be reduced to ISO5 (class 100) level by installing filter fan units and moving the machine into a ISO6 cleanroom cell. The contamination on a 6” substrate wafer went down to 15 pt./h in a pick-and-place test cycle.

![Figure 3: View on the C2W bonding interface - in the project, the actually available ASIC was smaller than the MEMS, so we used two die areas (gray areas) of the CMOS wafer for one single MEMS (only sealframe, Vernier and contact bumps are visible). The active ASIC is at right.](image)
Both wafers are prepared in advance with interface structures for gold-tin (Au-Sn) bonding. On ASIC side, this implies electroplating of a gold sealframe, contact bumps and the required signal routing from the MEMS contact positions to the ASIC pads (Figure 3, Figure 4).

Pre-conditioning of MEMS wafers for C2W

Before a single-die handling and bonding of MEMS was possible, many modifications of the standard flow had to be realized. We applied an approved surface micromachining process with 11 µm polysilicon as the proof mass layer on top of a sacrificial oxide, a thin buried polysilicon layer and an initial oxide [1]. The actual resonator measures only 1 x 1 mm² and is placed in a corner of the 3 x 3 mm² MEMS area (incl. sealframe). Additional structures allow to determine inherent stress in the polysilicon.

The device structures are defined by creating an oxide hardmask in frontend lithography. This allows to proceed with photosist-based structuring in our microsystems cleanroom area, where electroplating of gold and tin structures is performed. After the metallic interface definition, the MEMS resonator is formed by deep reactive ion etching (DRIE). The hard mask is removed in the sacrificial oxide etching. Throughout all these operations, the Au-Sn stack remains covered with photoresist to avoid metallic contamination of etching chambers. It is particularly important to avoid high temperatures that would lead to premature interdiffusion of Au and Sn, since otherwise no liquid metal phase will be available for final bonding.

Vertical design of the Au-Sn interface

Due to temperature limitations in post-CMOS processing, we decided for Au-Sn bonding as interconnect technology. The metallurgy is well known, yet we have two particular constraints in our approach: Primarily, we target a thin bondline below 20µm, which means that the interdiffusion zone must be very shallow. This has impacts on the bonding temperature profile, as we will see later. Second, we need to maintain a 2.4 µm gap between the dies for vacuum pumping. This can be reached by higher "prefixation bumps" that will collapse due to a partial liquefaction in final bonding. We placed the Au-Sn prefixation bumps in each corner of the MEMS cavity.

The die-bonder uses an ultrasonic tool to attach the devices on the corresponding Au pads of the substrate wafer. Parameter and tool adjustment is quite sensitive; rotational displacements and bad adhesion were frequent in the first attempts, but could be controlled later. Nevertheless we noticed that our initial 2 µm height offset between prefixation bumps and the other structures was insufficient and increased it to 4 µm in the next process lot.

Vertical design of the Au-Sn interface

Due to temperature limitations in post-CMOS processing, we decided for Au-Sn bonding as interconnect technology. The metallurgy is well known, yet we have two particular constraints in our approach: Primarily, we target a thin bondline below 20µm, which means that the interdiffusion zone must be very shallow. This has impacts on the bonding temperature profile, as we will see later. Second, we need to maintain a 2.4 µm gap between the dies for vacuum pumping. This can be reached by higher "prefixation bumps" that will collapse due to a partial liquefaction in final bonding. We placed the Au-Sn prefixation bumps in each corner of the MEMS cavity.

The die-bonder uses an ultrasonic tool to attach the devices on the corresponding Au pads of the substrate wafer. Parameter and tool adjustment is quite sensitive; rotational displacements and bad adhesion were frequent in the first attempts, but could be controlled later. Nevertheless we noticed that our initial 2 µm height offset between prefixation bumps and the other structures was insufficient and increased it to 4 µm in the next process lot.

The die-bonder uses an ultrasonic tool to attach the devices on the corresponding Au pads of the substrate wafer. Parameter and tool adjustment is quite sensitive; rotational displacements and bad adhesion were frequent in the first attempts, but could be controlled later. Nevertheless we noticed that our initial 2 µm height offset between prefixation bumps and the other structures was insufficient and increased it to 4 µm in the next process lot.

This allows to proceed with photosist-based structuring in our microsystems cleanroom area, where electroplating of gold and tin structures is performed. After the metallic interface definition, the MEMS resonator is formed by deep reactive ion etching (DRIE). The hard mask is removed in the sacrificial oxide etching. Throughout all these operations, the Au-Sn stack remains covered with photoresist to avoid metallic contamination of etching chambers. It is particularly important to avoid high temperatures that would lead to premature interdiffusion of Au and Sn, since otherwise no liquid metal phase will be available for final bonding.

Vertical design of the Au-Sn interface

Due to temperature limitations in post-CMOS processing, we decided for Au-Sn bonding as interconnect technology. The metallurgy is well known, yet we have two particular constraints in our approach: Primarily, we target a thin bondline below 20µm, which means that the interdiffusion zone must be very shallow. This has impacts on the bonding temperature profile, as we will see later. Second, we need to maintain a 2.4 µm gap between the dies for vacuum pumping. This can be reached by higher "prefixation bumps" that will collapse due to a partial liquefaction in final bonding. We placed the Au-Sn prefixation bumps in each corner of the MEMS cavity.

The die-bonder uses an ultrasonic tool to attach the devices on the corresponding Au pads of the substrate wafer. Parameter and tool adjustment is quite sensitive; rotational displacements and bad adhesion were frequent in the first attempts, but could be controlled later. Nevertheless we noticed that our initial 2 µm height offset between prefixation bumps and the other structures was insufficient and increased it to 4 µm in the next process lot.
Dicing of open MEMS wafers: The Mahoh process

If open MEMS are to be placed as dies on a CMOS wafer, they have to be singulated without damaging and contaminating the fragile microstructures. We investigated the ablation-free “Mahoh” stealth laser dicing process, which is known for its high dicing speed on thin wafers, mainly RFID products with more than 20,000 dies per wafer.

MEMS singulation is however not targeting for high speed: Our main interest lies in a particle-free separation of the components and we can easily accept twenty scan passes per scribe line. The actual dicing is made in a tape expansion step after the laser irradiation. We obtained excellent results even on thick wafers with up to 675 µm, under the condition that the dicing lanes be of sufficient width (>40% of the wafer thickness) and free of polysilicon and any reflective or absorbing layers along the full length, including the wafer borders. This may be obvious, given the nature of the laser beam and the way it is focused into the crystal, but has to be communicated to design and engineering responsibles. A more detailed report on the physical effects is given by Lange et al. [2]. The figure below illustrates well how the material transformation in the scan paths looks like.

IV. POST-PROCESSING OPTIONS FOR THE CMOS-WAFER

The "DAVID vision" shown in Figure 1 includes further technological features: A getter film, for example, can be integrated to guarantee a controlled lifetime vacuum level. For wafer-molding, TSVs can be used to access a backside contact array in form of solder balls. The wafer transfer molding is an interesting technology not only for C2W, but for all kinds of wafer products since no leadframe or other substrate is needed. This section reports briefly about these three additional components of the DAVID project.

Through-Silicon Via technology for thick wafers

Our TSV approach for the C2W concept is a post-CMOS process that we developed for thick wafers, i.e. 300 µm and above, to reduce the risk of fracturing and to comply with most industrial handling equipment.

For an acceptable via pitch, the diameters are in the 50..100µm range, so we developed the DRIE process to obtain an etching profile with strictly vertical sidewalls. Electrical conduction is made through a copper layer; the finished vias remain hollow to reduce the risk of fracturing the wafer. A later fill with elastic, low-CTE material could be part of a final packaging step; we even reached a good filling in our transfer molding process.

A so-called spacer-etch process is applied using silicon nitride deposition and subsequent anisotropic etching to open the pre-metal dielectric underneath the frontside pads. Further etching techniques are necessary that will be described in future publications. The insulated sidewalls are covered with copper in a MOCVD process, allowing approximately 1 µm thickness. With an additional electroplating, the resistance of feedthroughs can be further improved.
Thin-film getter deposition and structuring

In Figure 1, a black layer on top of the CMOS device is sketched to adumbrate a getter film that perfectly fits under the pads and it is favorable to use a uniform Metal-1 area as contact plane for the backside process. This type of pad design is a former state of the art, yet it was generally replaced by mosaic-like structures in most products for enhancing pad robustness.

We performed additional investigations on process and material compliance with CMOS integrated circuits. A significant number of devices was tested by electronic wafer sort equipment, before and after the deposition step and after getter activation. No impact on the wafer yield was found.

Outgassing from the CMOS wafer appears to be a critical subject: Argon, a non-getterable gas, is generally used as a process gas for sputtering metal layers. Even though most of the metal structures are embedded in oxides, solid state diffusion brings Ar atoms to the surface and into the cavity volume. Exposed metal areas like contact pads show strong outgassing, even after a long degassing cycle at 300°C. We observed that a thick passivation oxide on top of the CMOS wafer efficiently forms a barrier against Ar, and even outgassing of the very mobile hydrogen from the bulk volume is delayed.

Wafer molding and solder balling for chip-size systems

The proposed C2W implementation allows to form hermetically closed packages with frontside wirebonding capability on the ASIC. It can be used for wirebonding in packages like QFN or LGA, to form very small devices.

Using the TSV process allows to go further in the integration by placing a solder ball contact array on the backside of the ASIC. With this interface to the "outer world" it is principally possible to handle the device with conventional surface-mount equipment. Underfilling, glob-top or other additional steps would enhance mechanical robustness. However, our target is to provide stable operating conditions for the device over lifetime and to protect it against rough handling in manufacturing lines.

Transfer molding is the most proven technology for final packaging, even of very thin devices. Mold compounds are optimized for surface adhesion on microelectronic devices and provide well-balanced elasticity and thermal expansion properties. They also form a mechanical buffer between silicon and organic or metallic substrate materials. Compared to compression molding, the process cycle time for transfer molding is very short.

Nevertheless, this process was not applied on full wafer before and extensive studies on material properties and processing techniques were required. We started our work with long bimaterial strips of silicon and commercial mold compounds, forming samples of up to 200 mm length. Deflection measurements were used to establish simulation models of increasing complexity that helped to study some basic aspects of our targeted integration, and in particular to formulate material requirements for large area molding through a thin gap.

Currently, a new 6" wafer mold and a selection of specific mold compounds are being tested. We expect a significant reduction of wafer warpage from the patented "Dynamic Temperature Control" process: Rather than keeping the mold at a constant temperature, it is cooled down for curing the polymer matrix.

Nevertheless it is still recommended to design the system in a symmetric way to balance the stress on both sides of the wafer. A first study on a large sample with solder balls on one side and dummy dies on the other showed that warpage can be minimized in this way. A perfect matching of MEMS thickness and solder ball diameter may however become difficult in some actual system configurations.
To access contact pads in this configuration, either TSV through CMOS or a window opening in the MEMS can be used. Due to its much higher compactness, the TSV solution was studied, with special focus on throughput and yield in high volume manufacturing.

In this approach, the permanent wafer bonding of the MEMS to the ASIC is the first step, which allows backgrinding of the ASIC wafer to below 100µm thickness without a carrier concept. High-rate DRIE is performed to create cylindrical holes.

The full process is comparable to the C2W via processing, except that the metallization is made by electroplating on a thin, sputtered seed layer. Backside structures are defined in a spray-coated resist that allows lithography on our deep structured surface (Figure 16).

VI. CONCLUSION

We investigated several key technologies for waferlevel packaging of inertial MEMS devices, using a direct face-to-face bonding on CMOS wafers. Two complementary approaches, C2W and W2W, were described. A particular emphasis was put on the C2W implementation and some optional features: Post-CMOS via technology allows to create a backside solder ball array. Transfer molding of fullsize wafers represents a cost-optimized way to obtain extremely small packages. For the integration of resonant MEMS structures, a long-term vacuum level can be adjusted by means of fine-structured getter films. Deposition of these on top of CMOS wafers was demonstrated. Problems due to outgassing can be resolved and no functional interference with electronic circuits was found. In some aspects of our work, a convergence of C2W and W2W processes was observed that may lead to reduced cost and time for launching products based on the system integration concepts that we presented here.

ACKNOWLEDGMENT

We thank Accretech Tokyo Seimitsu for the Mahoh laser dicing, showing exciting perspectives for MEMS singulation. Furthermore, we thank Ramona Ecke from Technical University of Chemnitz for setting up the MOCVD process.

REFERENCES